A Novel Baseband-1.5 GHz Monolithic HBT Variable Gain Amplifier with PIN Diode Gain Control

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ABSTRACT

This paper reports on a GaAs HBT Variable Gain Amplifier (VGA) which monolithically integrates a GaAs PIN diode as a variable resistor to achieve wide gain control. The PIN diode is made from the intrinsic MBE layers of the HBT collector-base junction which consists of a 7000Å thick i-region. The novel VGA topology employs active feedback and output buffering to obtain high IP3 performance and is the first PIN-HBT VGA reported of its kind. The VGA obtains 10 dB gain and over 25 dB of gain control range at 1 GHz. The output IP3 is 15.1 dBm and the noise figure is 9.3 dB at maximum gain. The corresponding input IP3 is +5.1 dBm and remains constant over gain control which is an attractive feature of the HBT-PIN VGA. The PIN diode VGA design is realized in a miniature 0.8x0.4 mm^2 area. Integrated with a previously developed HBT LNA[1], the resultant low noise VGA MMIC demonstrates 2.1 dB noise figure, > 35 dB gain, +13.5 dBm OIP3, and over 25 dB of gain control at 1 GHz.

I. Introduction

Variable gain amplifiers are needed in many receiver applications for adjusting the input power of the received signal. For frequency applications from baseband to 2 GHz, a monolithic VGA is very attractive. At these frequencies, there is usually a compromise between performance and integration complexity. In order to achieve maximum performance for a given dc power, cumbersome off-chip components need to be integrated, especially at these frequencies. On the other hand, monolithic IC techniques offer a compact solution, but normally at the expense of higher dc power and lower performance. By integrating a GaAs HBT PIN diode as a variable series feedback resistance, a wide gain control VGA can be achieved in a compact chip which consumes little dc power. The resulting VGA is attractive for commercial wireless applications.

We have previously demonstrated various HBT VGAs [2],[3],[4] with different gain control techniques. A bias controlled VGA[2] and a parallel PIN diode VGA[4] had maximum gain control ranges which were limited to 15 dB. An analog current steering VGA[3] had excellent gain control which exceeded 35 dB, however, this topology required ≈ 700 mW (5V) of dc power and consumed a large area of 2.4x1.6 mm^2. A Si-BJT current steering VGA implementation achieved similar gain control performance as the HBT current steering VGA, but is limited to frequencies < 850 MHz and suffers from a similar size disadvantage[5]. The present work reports on a VGA which uses a GaAs PIN diode as a variable series feedback resistor to achieve > 25 dB of gain control from 0.05-1.5 GHz. Furthermore, the VGA is realized in a compact 0.8x0.4 mm^2 area and consumes less than 30 mA through 7V. In addition, active techniques are employed to improve the linearity performance without significantly impacting size. A unique characteristic of the PIN-VGA is that the input IP3 is constant over gain control. The novel VGA topology offers an attractive combination of low dc power, small size, and state-of-the-art gain control performance down to baseband frequencies.

II. Variable Gain Amplifier Design

The amplifier was fabricated using TRW's GaAs HBT baseline (foundry) IC process which has been described previously [4]. Fig. 1 shows the schematic of the HBT VGA which incorporates GaAs PIN diodes made from the collector-base layers of the HBT MBE structure. Transistor q_1 is a 2x10 μm^2 quad-emitter and provides the gain of the amplifier. A current mirror consisting of transistors q_2 and q_4, and resistor R_{ref}, provide the bias to q_1. For a given bias current of transistor q_1, the output swing is determined by the resistive load, R_{load}, and any impedance loading down the collector output of transistor q_1. In the absence of transistors q_3 and q_7, the collector of q_1 is loaded down by the 50 Ω system impedance as well as the feedback resistor R_{f1}. In order to obtain more output capability and higher IP3, either the quiescent current, or the load resistor R_{load}, must be increased. This however increases the voltage drop across R_{load} and increases the required supply voltage V_{cc}. In order to maintain a low supply

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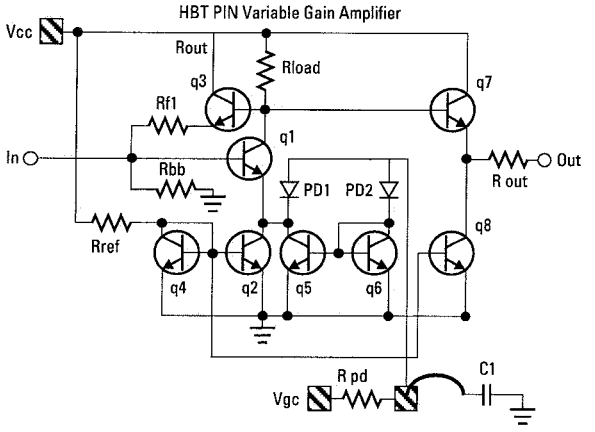


Fig. 1 Schematic of the HBT VGA.

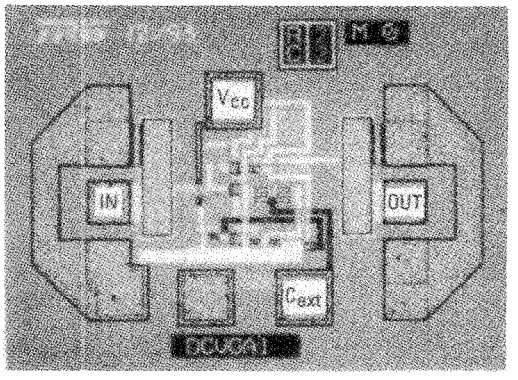


Fig. 2 Microphotograph of the HBT PIN VGA.

voltage, active feedback and output buffering transistors q_3 and q_7 are implemented to provide a high collector impedance. This results in higher IP3 for a given supply voltage and quiescent bias current.

Resistor R_{f1} provides parallel feedback while R_{bb} completes the biasing network for the base of q_1. Transistor q8 is a current source mirror for biasing q_7, the output follower. Resistor R_{out} helps provide output matching to 50 Ω. The emitter of transistor q_1 is coupled to ground through PIN diode PD1 and an off-chip die capacitor, C_1. A biasing network comprised of PIN diode PD2, transistors q_5 and q_6, and resistor R_{pd} are used in order to provide current bias to PIN diode PD1. As a control voltage V_{gc} is increased, the diode current of PD1 increases and the dynamic resistance of the diode drops (less feedback) which results in increased gain. The biasing network is needed to ensure that current provided through PD1 is not subtracted from the quiescent bias of q_1, the amplifying transistor.

Fig. 2 shows a microphotograph of the HBT PIN VGA. The chip is 0.8x0.4 mm^2. The active components consume only a fraction of this area. Only 1 off-chip die capacitor is required to complete the ac ground of the series feedback. This minimizes the number of parts to only 2 components, one being the MMIC.

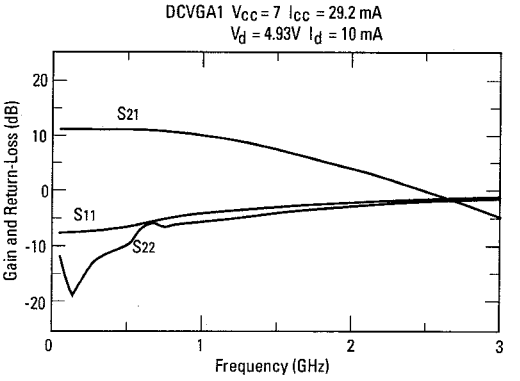


Fig. 3 Wideband gain and return-loss at maximum gain setting.

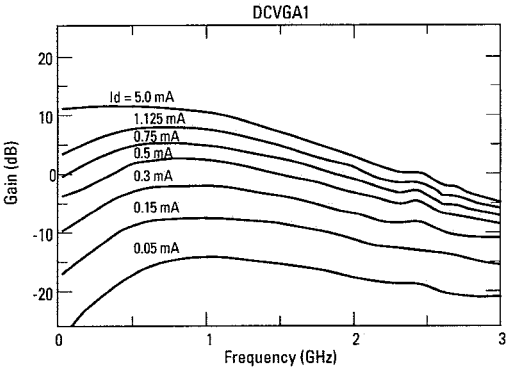


Fig. 4 Wideband gain response for various gain settings.

III. Measured Results

The HBT VGA described above was fabricated and measured on-wafer using custom probes which provide the off-chip ac-ground. Fig. 3 shows a wideband sweep (50 MHz to 3 GHz) of the gain and return-loss at maximum gain setting. The nominal gain is 11 dB with a 3-dB bandwidth of 1.5 GHz. The input and output return-losses are 8 dB and > 12 dB at 50 MHz, respectively, and degrade slowly with increasing frequency. Fig. 4 shows the wideband gain response for various gain settings. The corresponding PIN diode quiescent current is also given. As the PIN diode bias is increased from 0.05 mA to 5 mA, the gain changes from -14 dB to 10 dB at 1 GHz. This is a gain control range of ≈ 25 dB. At 50 MHz, the corresponding gain control is > 35 dB. This is because the series impedance of the PIN diode consists predominantly of the dynamic resistance at lower frequencies. At high frequencies the dynamic resistance becomes bypassed by the dynamic diffusion capacitance, reducing the effective resistive impedance range.

In order to obtain higher IP3, active feedback and output buffering of the collector of q_1 were implemented. The IP3 and gain performance of the amplifier were measured and compared to an equivalent amplifier which did not include the collector buffering. Fig. 5 shows gain at 1 GHz versus quiescent bias current of PIN

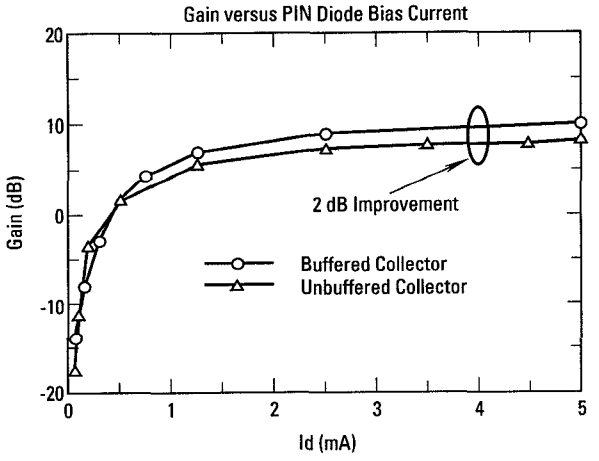


Fig. 5 Gain at 1 GHz versus quiescent bias current of PIN diode PD1, for the buffered and un-buffered VGAs.

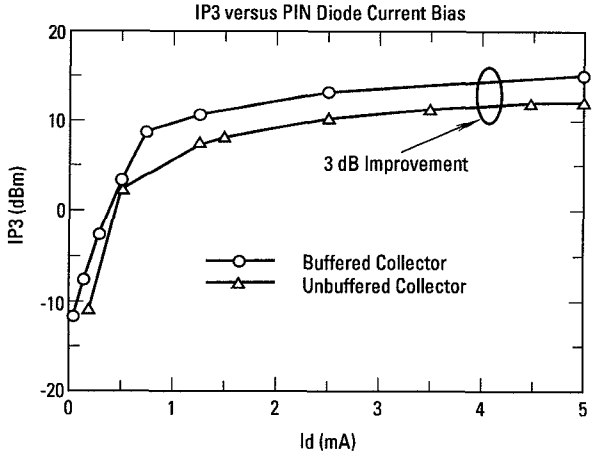


Fig. 6 IP3 at 1 GHz versus quiescent bias of the PIN diode for the buffered and un-buffered VGAs.

diode PD1 for the two amplifiers. The curves indicate that there is a 2 dB improvement in gain of the buffered output design. Fig. 6 shows the IP3 at 1 GHz versus quiescent bias of the PIN diode for both amplifiers. An approximate improvement in IP3 of 3 dB is observed for the buffered collector design. This design only consumes twice the dc power of the conventional un-buffered design.

For VGAs, the behavior of the IP3 and noise figure over gain control determines the lower limit of the dynamic range. Fig. 7 reveals the IP3 and noise figure performance plotted versus amplifier gain at 1 GHz. The IP3 versus gain shows a linear relationship where the IP3:gain slope is ≈1:1. At maximum gain the IP3 is 15.1 dBm. The corresponding input IP3 is 5.1 dBm and is constant over gain control. A slope of 1:1 or less is desirable for VGAs in order to maintain a constant input IP3 over gain control. Previous VGAs have been characterized by a slope of > 1.5:1[2] which means the input IP3 and dynamic range decreases with gain

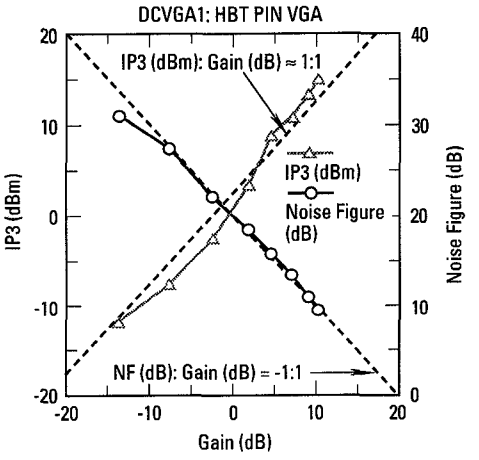


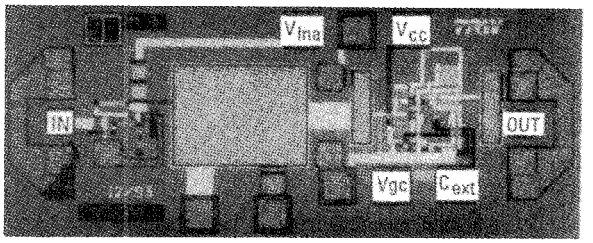
Fig. 7 IP3 and noise figure characteristics plotted versus amplifier gain.

control. The use of PIN diode gain control results in significant performance improvement.

The noise figure versus gain characteristic is also revealed in Fig. 7. This plot shows that the noise figure is also linearly related to the gain and has a slope of -1:1, which is a highly desirable feature of the VGA. For incoming received signals which are small, high gain and low noise figure is desirable. For larger signal strengths, the signal to noise ratio is better and does not require as low a noise figure.

IV. Low Noise VGA MMIC

The VGA was integrated with a previously developed HBT LNA[1] in order to achieve lower noise and higher gain performance. A microphotograph of the chip is shown in Fig. 8a. The MMIC is compacted into a 1.54x0.63 mm^2 area. Fig. 8b gives the corresponding block diagram and gain budget of the MMIC. The HBT LNA operates from dc to 4.5 GHz and has 24.6 dB gain with a noise figure ranging from 2.0-2.5 dB. It is biased through a 7 Volt supply and draws10.6 mA of current, but can also operate through a 5V or 3.5 V Supply. The LNA stage is AC-coupled to the PIN VGA stage whose performance is also summarized. The resultant MMIC has a bandpass response from 150 MHz to 1.5 GHz with a max. gain of 35.6 dB. The noise figure and IP3 at max. gain are 2.2 dB and 13.5 dBm, respectively. Fig. 9 is a plot of IP3 and noise figure versus gain at 1 GHz. This plot shows that the NF:Gain and IP3:Gain slope characteristics remain ≈ -1:1 and 1:1, respectively, with the HBT preamplifier cascaded in front of the PIN VGA. These results suggest that the unique performance features of the PIN VGA topology can be preserved in a cascaded amplifier chain, which is itself another attractive feature of the buffered collector design.



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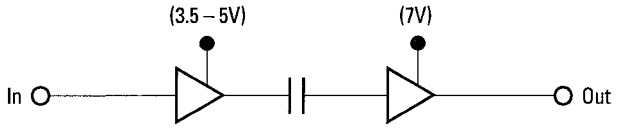

	LNA	Pin VGA	Total
Freq	dc – 4.5 GHz	dc – 1.5 GHz	0.15 – 1.5 GHz
Gain	24.6 dB	11 dB	35.6 dB
IP3	7.5 dBm	15 dBm	13.5 dBm
NF	2.1 dB	9.3 dB	2.1 dB
Icc	10.6 mA	29.2 mA	39.8 mA

b)

Fig. 8 a) Photograph of the integrated LNA-VGA MMIC. The chip is 1.54x0.63 mm^2 in area, b) corresponding block diagram and gain budget.

V. Conclusion

This work demonstrated a 50 MHz to 1.5 GHz GaAs HBT VGA which achieved > 25 dB of gain control using a GaAs HBT PIN diode as a variable series feedback element. The design obtains 10 dB gain, an IP3 of 15.1 dBm, and a noise figure of 9.3 dB. The IP3:Gain and NF:Gain ratios were ≈ 1:1 and -1:1, respectively, and are linear across the gain control range. This characteristic of the PIN VGA topology enables wide dynamic range performance in receiver systems. By employing active techniques, a 3 dB measured improvement in IP3 was obtained. The VGA was realized in a miniature 0.8x0.4 mm^2 area resulting in a low cost chip component. Integrated with an HBT LNA, a low noise VGA with 2.1 dB NF, > 35 dB gain, +13.5 dBm OIP3, and 25 dB of gain control was demonstrated in a compact 1.54x0.63 mm^2 MMIC. The low dc operation, miniature cost, and high functional complexity in a compact area makes HBTs attractive for many commercial applications.

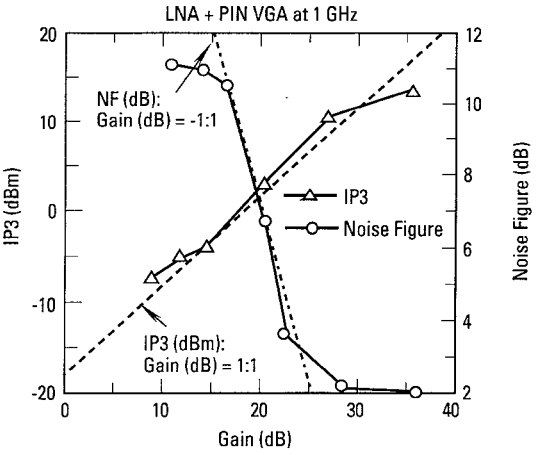

Fig. 9 IP3 and noise figure versus variable gain at 1 GHz.

Acknowledgment

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